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Code No. : 22616

VASAVI COLLEGE OF ENGINEERING (Autonomous), HYDERABAD
M.E. (ECE: CBCS) II-Semester Main Examinations, June-2018
(Embedded Systems & VLSI Design)

CPLD & FPGA Architectures and Applications

Time: 3 hours

Max. Marks: 60

Note: Answer ALL questions in Part-A and any FIVE from Part-B

Part-A (10 × 2 = 20 Marks)

1. Define PLD. Write the classification of PLDs.
2. List the applications of CPLDs and FPGAs in digital design.
3. List out any two comparisons among different programming technologies of FPGA.
4. Draw the general structure of FPGA and list out the major components.
5. Give the features of ALTERAs CPLD Max 7000 series.
6. Define CPLDs? Briefly outline salient features of these devices and applications.
7. Define Routing and also list out different routing algorithms.
8. Define critical path and brief it's importance in Placement and Routing.
9. List out any two commercial tools available for simulation and synthesis.
10. Describe stuck-at fault modeling with suitable example.

Part-B (5 × 8 = 40 Marks)

11. a) Draw and explain logic diagram of 16R8 PAL with an example. [5]
b) Compare EPROM, PLA, PAL Programmable Logic Devices. [3]
12. a) Draw a basic block diagram of Xilinx 3000 FPGA and explain briefly about CLB. [5]
b) Write a brief note on AMD FPGA. [3]
13. a) Explain Cypress FLASH 370 device technology in detail. Also compare it with ALTERA FLEX logic 10000series. [5]
b) Explain about Lattice PLSI structure. [3]
14. a) Explain about min-cut based placement and iterative improvement placement. [5]
b) Explain segmented channel routing algorithm. [3]
15. a) Compare the Architectural features of FPGAs & ASICs. [4]
b) Explain about BIST technique in testing FPGA's. [4]
16. a) Explain SRAM programming Technology. [4]
b) Discuss about Macrocell in detail with a neat sketch. [4]
17. Answer any *two* of the following:
a) Optimized Reconfigurable Cell Array (AT&T ORCA). [4]
b) Simulated Annealing. [4]
c) Programmability Failures. [4]